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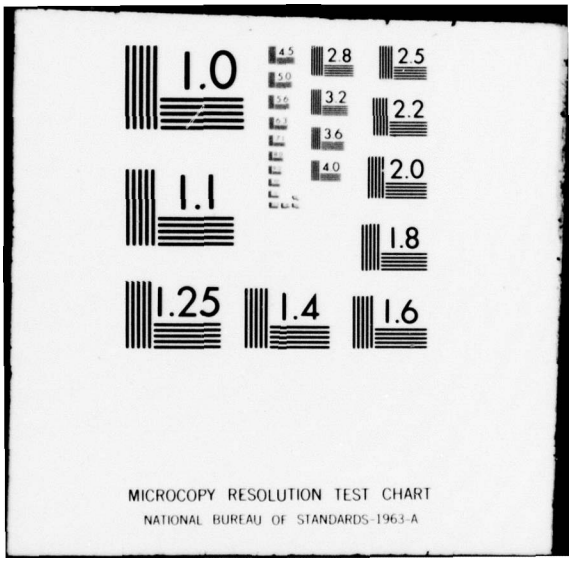
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Research and Development Technical Report
DELET-TR-77-2647-F

FLOATING DECK GRID MODULATOR

D. V. SAVAGE
HUGHES AIRCRAFT COMPANY
GROUND SYSTEM GROUP
FULLERTON, CA 92634

October 1978

Final Report for Period March 1977 to May 1978

Prepared for: US Army Electronics Technology & Devices Laboratory

ERADCOM

US ARMY ELECTRONICS RESEARCH AND DEVELOPMENT COMMAND
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Microwave Transmitter Components

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

The all solid state Floating Deck Grid Modulator has been completed and successfully tested. The design goals of pulse width, pulse amplitude, duty cycle, operation in a 50 KV gradient and circuit survival during multiple crowbars of the 50 KV power supply have been met. The rises and fall times are less than 700 nsec.

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ABSTRACT

The all solid state Floating Deck Grid Modulator has been completed and successfully tested. The design goals of pulse width, pulse amplitude, duty cycle, operation with a 50 kV gradient and circuit survival during multiple crowbars of the 50 kV power supply have been met. The rise and fall times are less than 700 nsec, and are limited by the pulse isolation transformer.

SUMMARY

The solid state Floating Deck Grid Modulator provides pulses of 1 to 12 μsec duration with less than 700 ns rise and fall times, and with the TWT positive grid to cathode amplitude adjustable from 700 volts to 1000 volts. During the interpulse period, the TWT grid is maintained at -1000 volts with respect to the cathode. High pulse fidelity is maintained, with a pulse overshoot of 2% and a pulse to pulse stability of .002%. The Modulator is also capable of operation at a 6% duty cycle with a 10-12 μs pulse width. In addition, the amount of circuitry that must "float" at the TWT cathode potential has been minimized, in order to improve both reliability and maintainability

FINANCIAL STATUS

Total Manhours – 3045
Total expenditures – $77,000

PROGRAM OBJECTIVE

This objective of this program was to develop a documented working model of a pulse transformer type TWT grid modulator with a block diagram as given in Figure 1 and with performance goals as given in Table 1. This particular configuration was chosen in order to minimize the amount of circuitry at the TWT cathode potential, and thus enhance reliability and maintainability. The pulse transformer secondary will drive the TWT grid directly while referenced to the -50 kV TWT cathode potential, while the primary of the transformer is driven by solid state circuitry operating at potentials ranging from 200 to 400 volts with respect to chassis ground. The secondary output is a 2 kV pulse to modulate the grid of a high powered TWT.

PROGRAM ORGANIZATION

The design portion of the program was accomplished in three separate phases corresponding to the three major design problems associated with a modulator of this type.

1. The transformer was designed to be able to continuously withstand a secondary to primary voltage stress of -50 kV DC and simultaneously exhibit a primary leakage inductance low enough to allow a secondary pulse rise time of 1 μsec maximum.

2. The primary drive transistors were chosen to operate at high peak power dissipations at high temperatures but without failures due to secondary

breakdown. The primary drive circuitry operates with current rise and fall times <0.5 μsec to charge and discharge the circuit stray capacity.

3. Since the pulse transformer must be under damped to provide the short rise and fall times required, it exhibits overshoot and ringing. The phase stability requirements of the TWT therefore result in the requirement for regulation of the grid pulse top. Active circuitry was designed to perform pulse top clipping and regulating functions and negative bias clamp functions. The design requirement outline is shown below for reference.

FLOATING DECK FUNCTIONS

A block diagram of the Floating Deck is shown in Figure 1. The primary side of the pulse isolation transformer is driven by an all solid state circuit. The drive circuits are referenced to ground potential and power is supplied to them by a separate 200 volt positive supply. The trigger pulses are transformer coupled to the driver circuits and are converted to power pulses, with sufficient power to drive the Pulse Isolation Transformer primary winding.

The pulse top clipper regulator is in the form of a closed control loop that both clips the oscillations on the modulator transformer secondary and controls the level of the TWT grid pulse across the width of the pulse.

Since interpulse negative grid voltage must only maintain the TWT in the off state and is not otherwise critical, the bias supply is shunt regulated by a series string of zener diodes. In addition, the clamp supply clamps the negative overshoot from the modulator transformer to a level within the rating of the TWT.

Power is provided to the floating deck by a power isolation transformer. One secondary of this transformer provides power to the TWT filament regulator, which in turn provides stable power at 8V and 10A to the TWT filament. The voltage from the other secondary of the transformer is rectified, filtered, and used to supply regulated 30 Vdc to 80 kHz inverters, which in turn provide power to the various circuit components on the floating deck.

The TWT filament fault circuit and the TWT grid bias fault circuit provide optical signals through fiber optic couplers from the -50 kV level to TPQ-37 transmitter control unit (TCU) interfaces at ground level. If either the TWT filament voltage or TWT grid bias voltage deviate from preset limits, an appropriate signal is transmitted to the TCU and system operation is terminated.

DESIGN REQUIREMENT OUTLINE

I. MODULATOR TRANSFORMER

- a. Input/Output Voltage Levels
- b. Driving Point Impedance (Rise Time)
- c. Voltage Isolation Capability
- d. Size, Weight

II. DRIVERS

a. GTO SCR
b. NPN Bipolar Transistors
c. PNP Bipolar Transistors

III. PULSE TOP CLIPPER

a. Amplifier
b. Control Element (Transistor)
c. Voltage Shifters (Zeners)
d. Input Circuits (Sensors)

IV. BIAS SUPPLY

a. Bias for TWT
b. Negative Clamp

V. INSTRUMENTATION

a. Filament Fault
b. Bias Fault

VI. POWER SUPPLIES

a. TWT Heater
b. 30 Vdc
c. 80 kHz Inverters

OVERALL MODULATOR PERFORMANCE

Breadboards of the pulse transformer, the driver circuit, the bias circuit, the clamp circuit, the pulse top regulator and the fault circuit were completed. The circuits were first tested individually, and then connected together and tested as a unit in the form of the block diagram shown in Figure 1. The completed modulator was then connected to a load that simulates the grid of the TPQ-37 TWT final amplifier as shown in Figure 2, with waveforms of the modulator output pulse shown in Figure 3. Figure 3a is the waveform of the pulse top taken at 10 volts per centimeter. The figure shows the overshoot which is about 20 volts (2%) above the pulse center level. The rise across the width of the pulse is characteristic of the shunt type clipper regulator. Figures 3b and 3c show the rise and fall times of the output pulse to be $<0.7\ \mu s$. Figure 3d is a photograph of the total pulse which shows the pulse rising from the bias level to the pulse top.

Figure 3e is the waveform of the center of the pulse top taken at 100 mv/cm. Since the exposure is the result of a repetitive waveform, the figure indicates that the pulse top is repetitive from pulse to pulse with vertical jitter on the order of 20 mv. This result is consistent with the specification requirement of .0025% pulse top stability. The pulse top regulator provides this necessary pulse stability, as well as permitting pulse amplitude adjustment from +700 volts to +1000 volts, while the bias circuit maintains the load at a negative 1 kV during the interpulse period.

Satisfactory operation was obtained at pulse widths between one and twelve microseconds, and at continuous duties up to 6% at the widest pulse widths. Table 1 summarizes the original design goals and the results achieved.

DETAILED CIRCUIT DESCRIPTION

The Pulse Isolation Transformer is the central and limiting component in the modulator design. After a preliminary design, the transformer equivalent circuit shown in Figure 5 was constructed for the preliminary tests of the driver circuits, where these tests indicated that the primary circuit power dissipations and pulse rise times would be reasonable. The "first cut" transformer design met the requirements for the completed modulator prototype. Two transformers were then constructed for test; one for low voltage tests to expedite the development, and a later unit with complete high voltage capability.

The modulator transformer is constructed on a core of 2 mil 80% Ni. The core geometry and material were selected to provide a 12 μsec pulse width with minimum pulse top droop. The transformer construction is shown in Figure 4. Each primary winding is made of 2 mil copper foil to achieve closer coupling and thus a lower leakage inductance. The secondary winding is No. 26 AWG magnet wire. The primary and secondary are insulated for a 50 kV voltage gradient with Kapton and Kraft paper. The start and finish turns of each of the secondary windings are made of 1/4" copper tubing to minimize the voltage gradient to the surrounding ground potential.

The transformer provides the characteristics shown in Table 1 when loaded with the equivalent TWT grid circuit shown in Figure 2. Since these parameters were adequate for the intended system purpose, as shown in Table 2, no effort was made to improve the rise time. However, the results indicate that rise times on the order of 0.2 μsec would not be unreasonable in a transformer of this kind. The high voltage transformer configuration was operationally tested with the completed modulator circuitry with a primary to secondary voltage stress of -50 kVDC while the transformer was immersed in liquid Fluorochemical FC78. The transformer did not exhibit any arcing or corona.

Three separate driver circuits were constructed to test with the transformer; a Gate Turn Off (GTO) SCR configuration shown in Figure 6 and two transistor configurations shown in Figure 7. The GTO unit was discarded because the gate leakage at high temperature could not be stabilized resulting in degradation of hold off capability with increasing temperature. Both transistor circuits worked well with the transformer but the NPN circuit was used for the final tests for the reasons given below. The circuit designs of Figure 7 are identical with circuit implementation differing only in power supply and semiconductor polarity reversals. The output transistors are driven on by a fast pulse coupled through the .082 μfd capacitor from the intermediate driver transistor. The output transistors are maintained in the on state for the remainder of the 10 μsec pulse by the input pulse transformer. Two driver circuits are used to operate the modulator transformer; one as an "on" driver and one as an "off" driver. One end of the "on winding" is connected to the 200 volt supply, while the other end is driven to ground by the "on driver". One end of the "off winding" is connected to ground and again the other end is driven to ground by the "off driver." Thus, the "off driver" effectively shorts the "off winding"

dissipating the energy stored in the transformer which in turn rapidly switches the output of the secondary winding to the off state. This primary configuration eleminates the typical application of doubled power supply voltage to the off state transistor and eases the collector voltage rating requirement. Figure 8a is a waveform photograph of the primary circuit current waveform. While Figure 8b shows the equivalent voltage. The combination of waveforms indicates that the "on driver" transistors dissipate a peak power of approximately 0.6 kW, the peak current is 11.0 amperes and the peak driver transistor voltage stress is 200 volts. Table 3 is a comparison of the driver transistor specifications and the actual operating characteristics. These results indicate that the NPN driver transistors in parallel operate within their capabilities and are not in any way overstressed. However, the PNP transistor peak current capability is not adequate for this design without paralling an unreasonable number of devices.

The pulse top clipper regulator shown in Figure 9 employs a feedback loop to set and maintain the desired pulse top voltage on the clipper capacitor. When the pulse transformer output rises above the clipper capacitor voltage, the clipper diode conducts and begins to charge the clipper capacitor to a higher voltage. Since the clipper capacitor is relatively large (.25 μfd) the charge rate during the pulse period only allows the pulse output to rise about ten volts. This pulse rise serves to offset the pulse droop exhibited by a pulse transformer. The modulator output excursion is thus limited by the clipper diode and capacitor. Voltage changes on the clipper capacitor are sensed by the compensated divider network, amplified and used to control the current through the DTS 804 and the series stack of 330 volt zener diodes. The zener diodes limit the collector voltage on the DTS 804 to a safe level (990 volts) and also bound the clipper control range between +1250 volts max and +660 volts min. The response of the clipper control loop need only be fast enough to restore the voltage level on the clipper capacitor during the relatively long interpulse period. This permits the control loop to closely set the voltage on the clipper capacitor at the start of each pulse, thus providing the required close control of the pulse to pulse voltage.

The negative bias voltage of -1 kV is applied to the TWT grid in series with the pulse transformer secondary winding. The pulse transformer output voltage is therefore set to +2 kV, to result in a maximum of +1 kV pulse amplitude. Both the bias supply and the clamp supply shown in Figure 10 are series strings of wide tolerance zener diodes which are powered from a common supply. The bias supply current drain is very low and is connected to the common source through a 30 K ohm resistor. The clamp supply must absorb the "backswing" energy from the transformer and is connected to the common source through 11 K ohm resistor. In addition, the clamp supply is connected directly to the transformer through the clamp diode which isolates the clamp supply from the positive output pulse.

The floating deck and TWT filament power supplies shown in Figure 11 are taken directly from the TPQ-37 system and perform the same functions in this application. The current drain on the 28 volt supply is approximately 5 amperes in the TPQ-37 system and about 2 amperes in this application. The TWT filament supply is used without modifications. The bias and heater fault sense circuits shown in Figure 12 are also the same as those used in the TPQ-37 system circuits, and perform identical functions.

CONCLUSIONS

The solid state modulator developed by this program satisfactorily performs the functions required by the TPQ-37 radar system. The design can be productized with no component overstress and with all Mil grade components. The reduced component count, particularly at the high voltage, should result in a significant increase in reliability. The transformer tests performed during this development indicate that closer coupling of the primary winding to the core and careful construction could result in 200 nsec rise and fall times. The transformer also could easily be made to provide 3 kV secondary pulses to accommodate the grid modulation requirements of a wider range of RF power tubes.

RECOMMENDATIONS

This modulator is compatible with the requirements of the TPQ-37 system and should be tested in an operating TPQ-37 transmitter. The only significant mechanical effort in conducting this test would be the fabrication of a pressure vessel to house the transformer. The remainder of the modulator is directly compatible with the TPQ-37 transmitter circuitry.

TABLE 1. MODULATOR PERFORMANCE OBJECTIVES

Function	Design Goal	Results Achieved
D.C. Bias	-1000 volts	-1000 volts
Pulse Amplitude	+1200 volts	+1250 volts
Load Capacitance	150 pf	150 pf
Load Impedance	500 K ohms	45 K ohms
Pulse Width	Variable 1-12 μsec	Variable 1-12 μsec
Duty Cycle	0.06	0.06
Pulse to Pulse Stability	0.0025%	0.002%
Pulse Top Overshoot	3%	2%
Pulse Rise Time 10-90%	250 nsec	<700 nsec
Pulse Fall Time 90%-10%	250 nsec	<700 nsec

TABLE 2. TPQ-37 MODULATOR PERFORMANCE REQUIREMENTS

Parameter	Symbol	Design Goal
Grid Pulse Rise Time	t_r	<1 μsec
Grid Pulse Fall Time	t_f	<1 μsec
Minimum Pulse Width	Tw	1 μsec
Maximum Pulse Width	Tw	12 μsec
Maximum Duty Cycle	D_{max}	5%
Pulse Top Overshoot	V_{pk}	10%
Pulse Top Stability	ΔE	0.0058% RMS Max

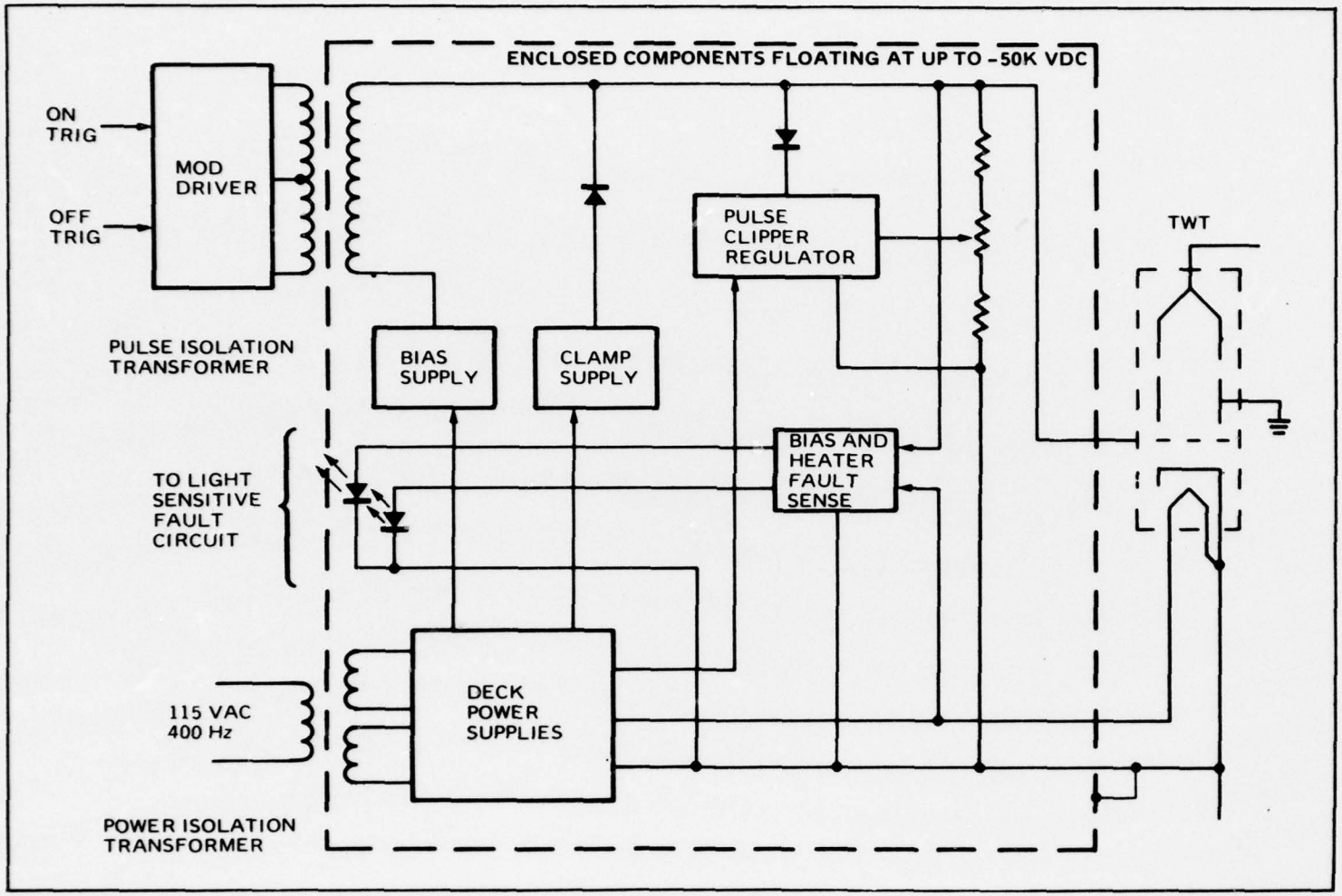


Figure 1. Floating Deck Block Diagram

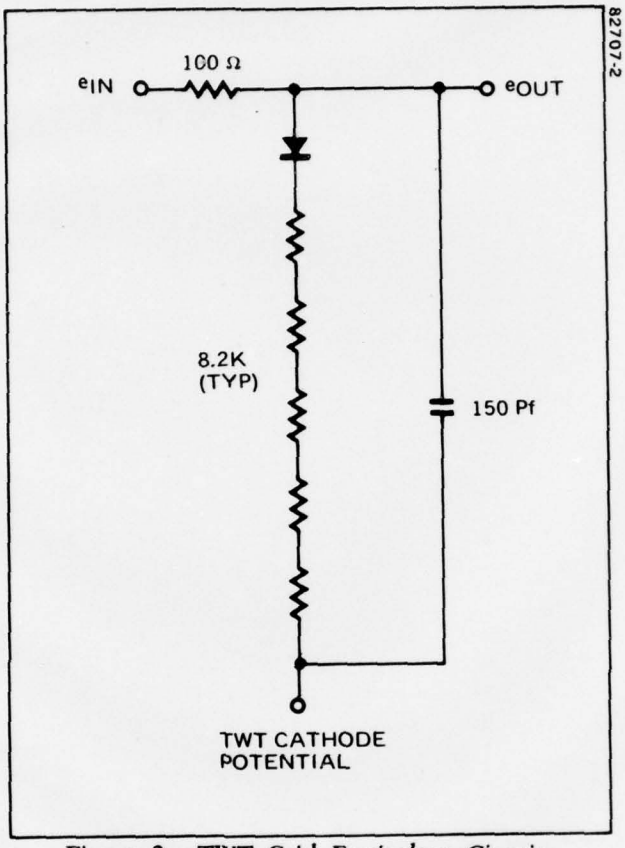


Figure 2. TWT Grid Equivalent Circuit

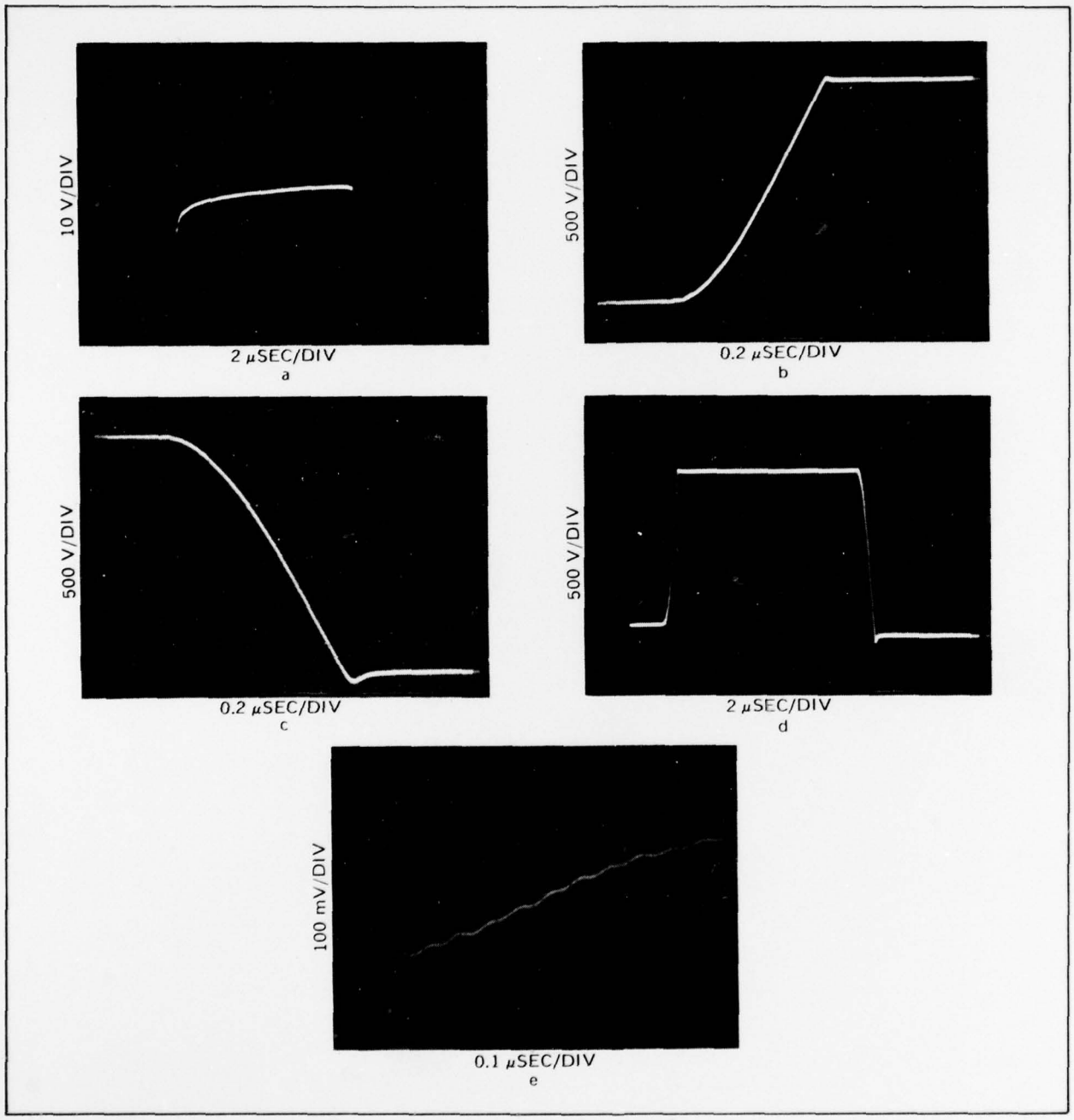


Figure 3. Output Pulse Waveforms

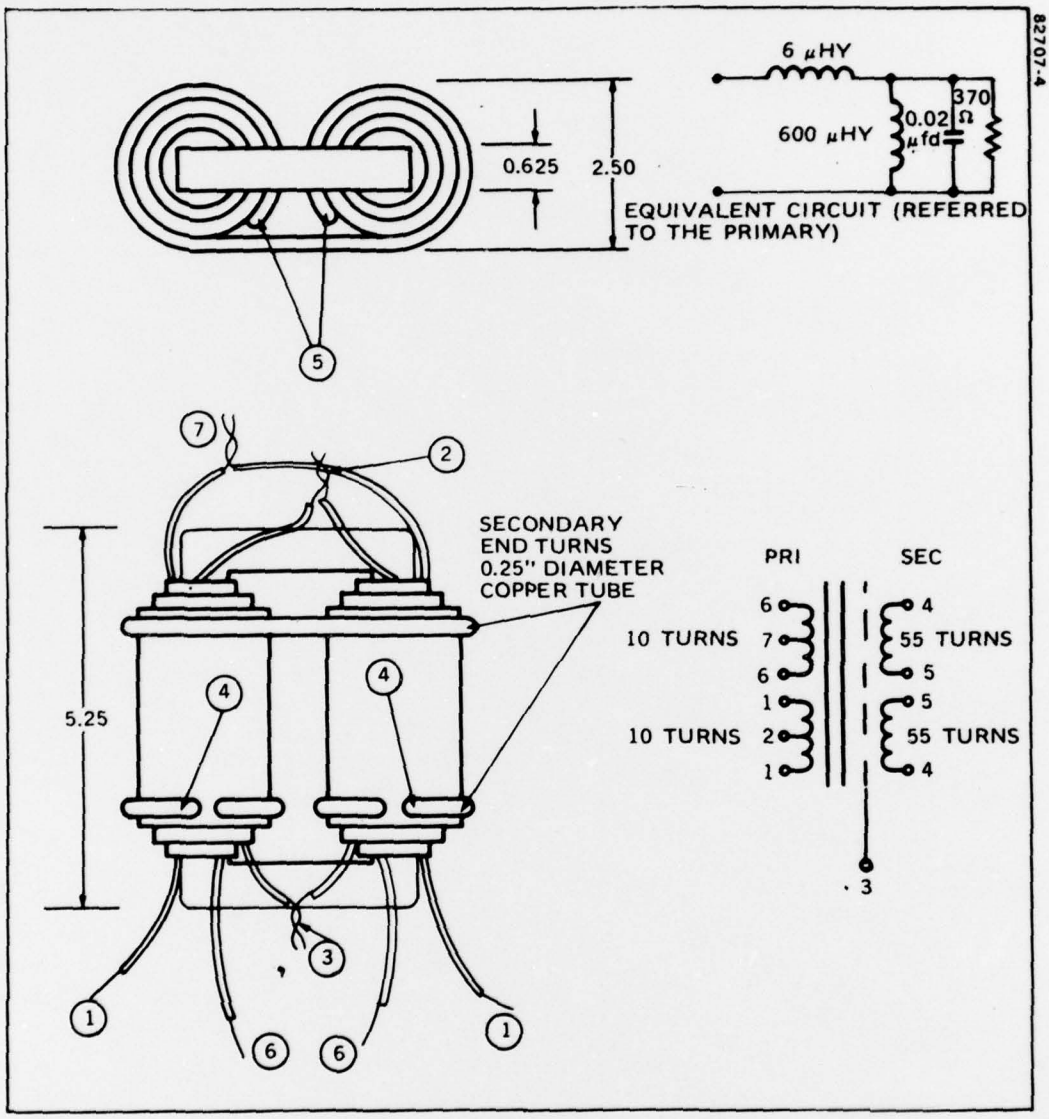


Figure 4. Modulator Transformer Construction

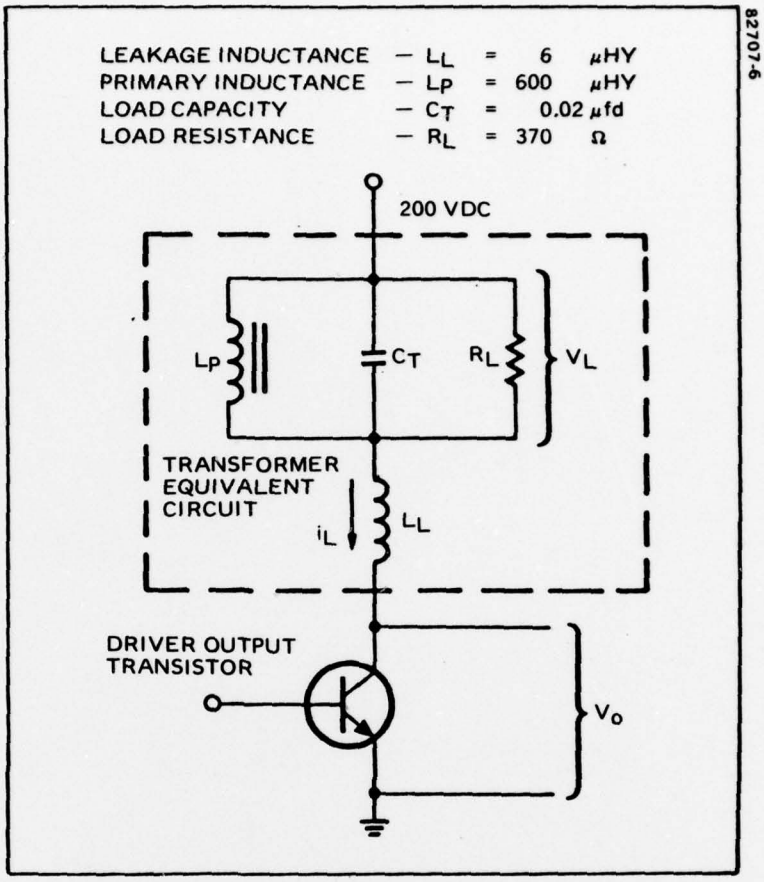


Figure 5. Modulator Transformer Equivalent Test Circuit

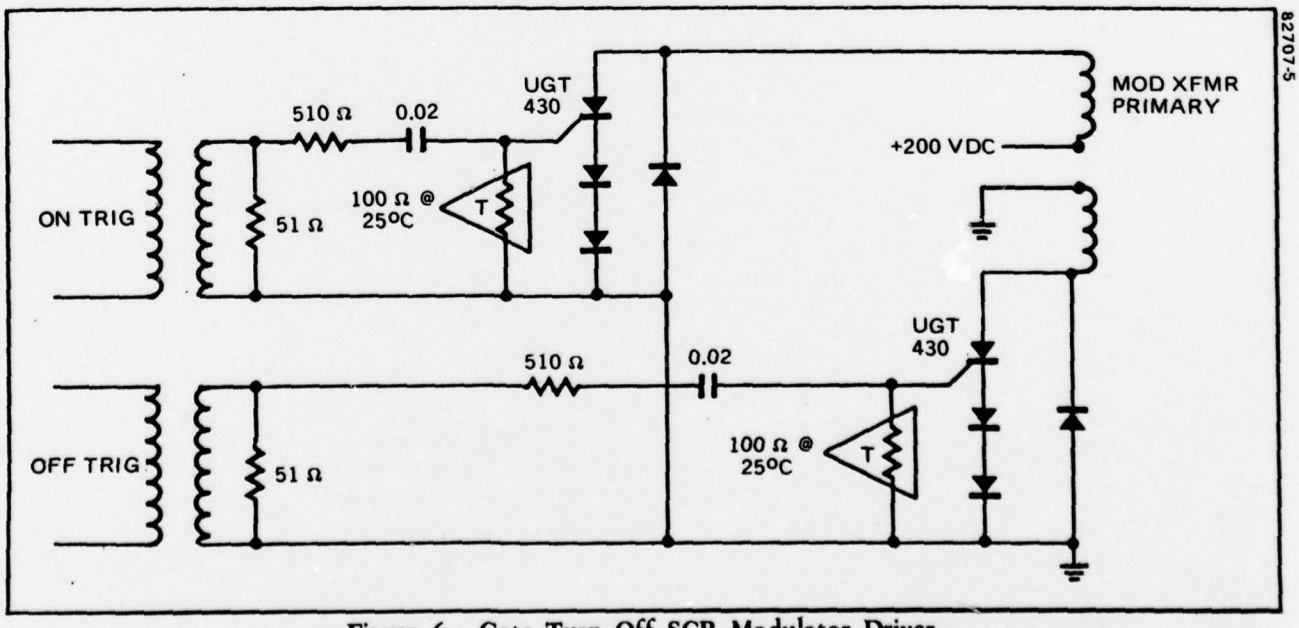


Figure 6. Gate Turn Off SCR Modulator Driver

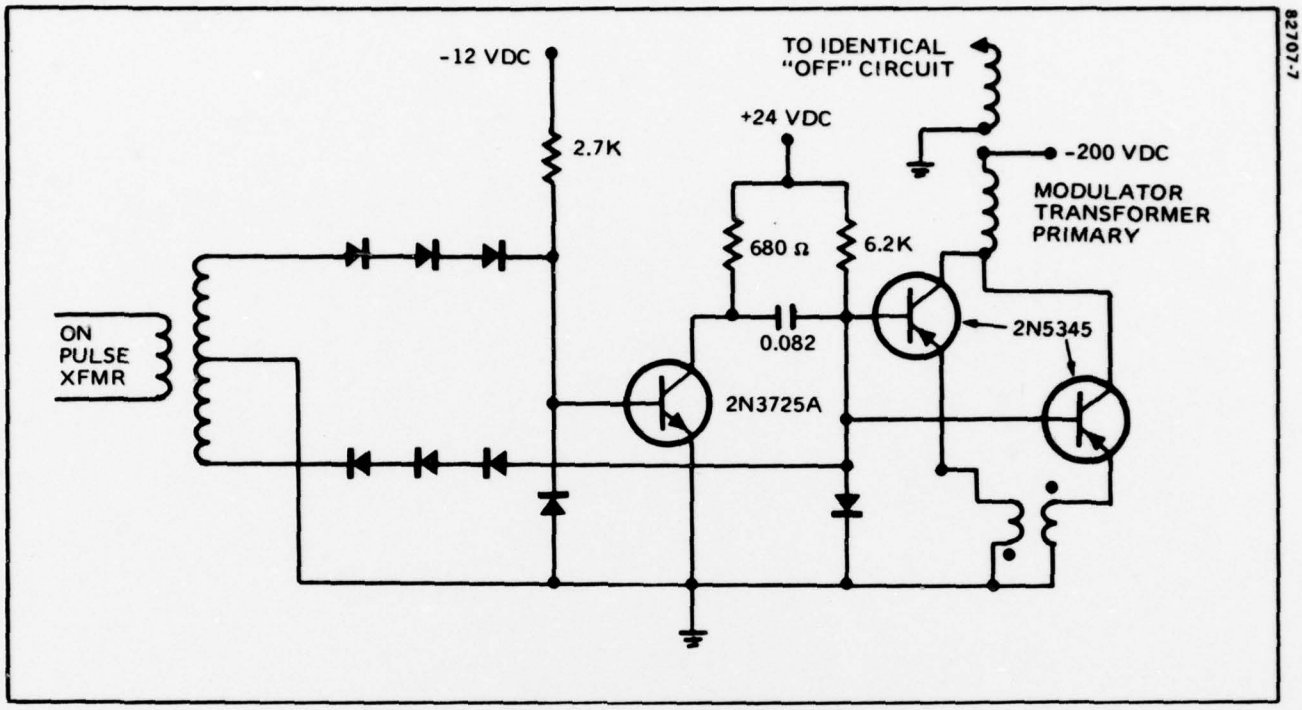


Figure 7a. PNP Transistor Modulator Driver

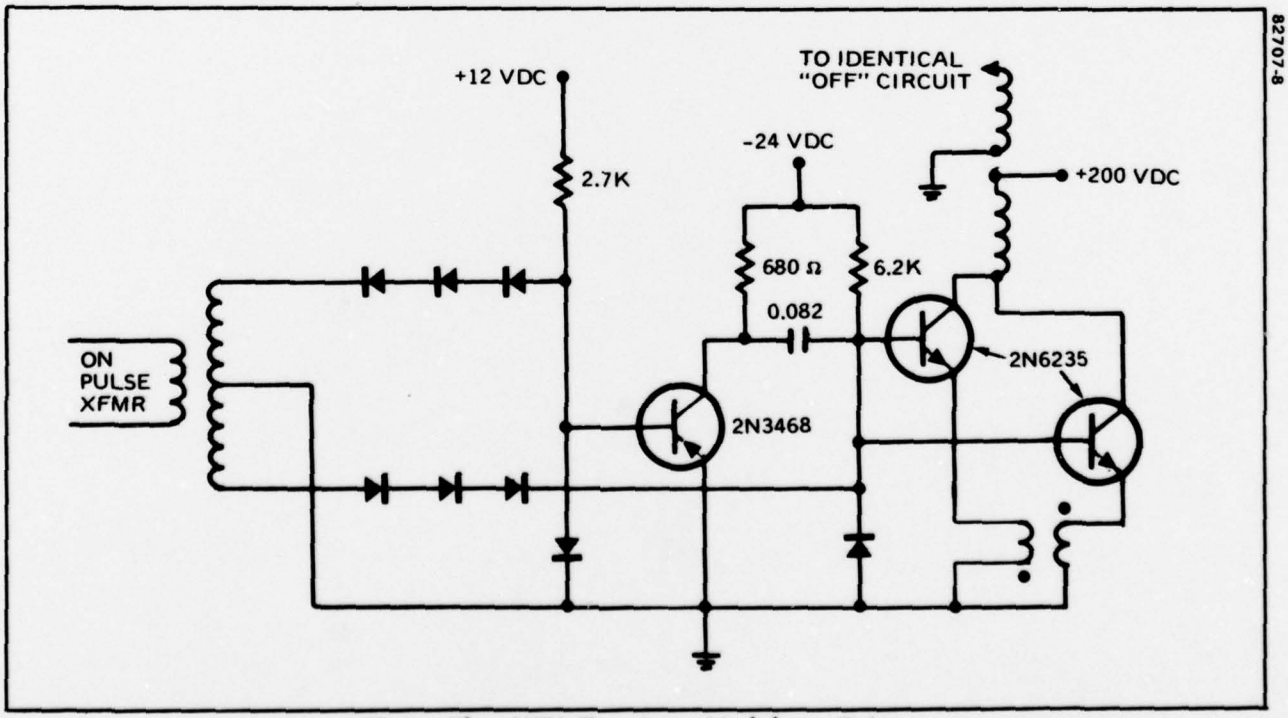


Figure 7b. NPN Transistor Modulator Driver

TABLE 3. TRANSISTOR PARAMETERS

Parameter	V_{CE}	I_{PK}	Avg Pwr
Operating Stress	200V	11A	3W
PNP Rated Stress (2N5345)	300V	2A	20W
NPN Rated Stress (2N6235)	325V	10A	25W

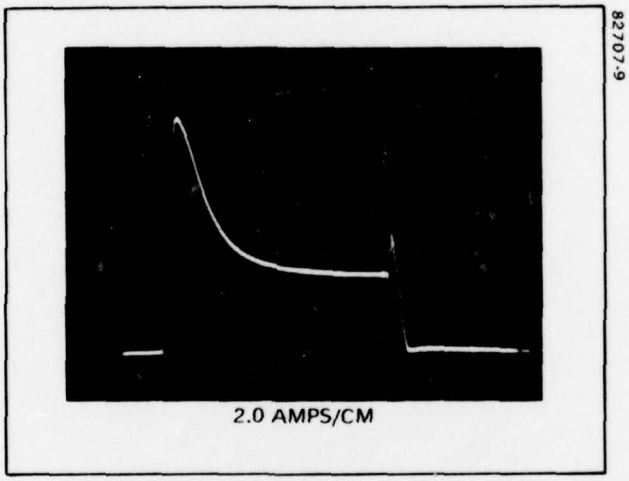


Figure 8a. "On" Driver Current

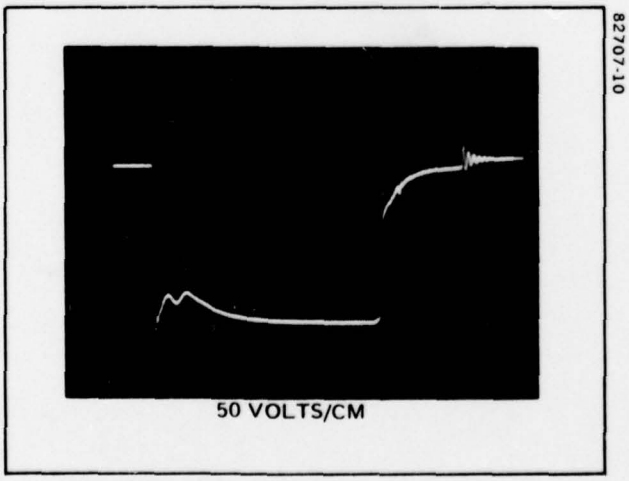


Figure 8b. "On" Driver Voltage

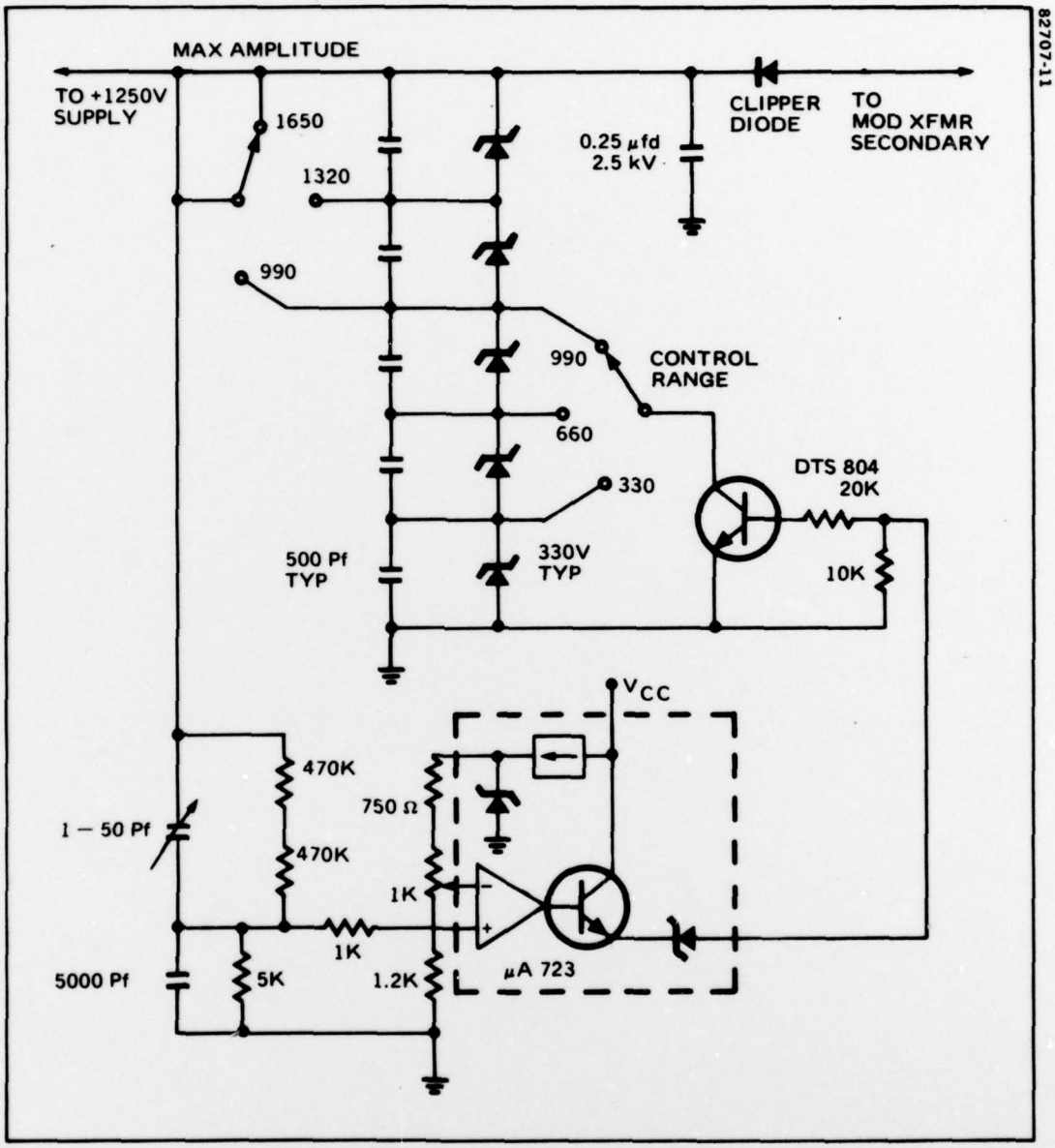
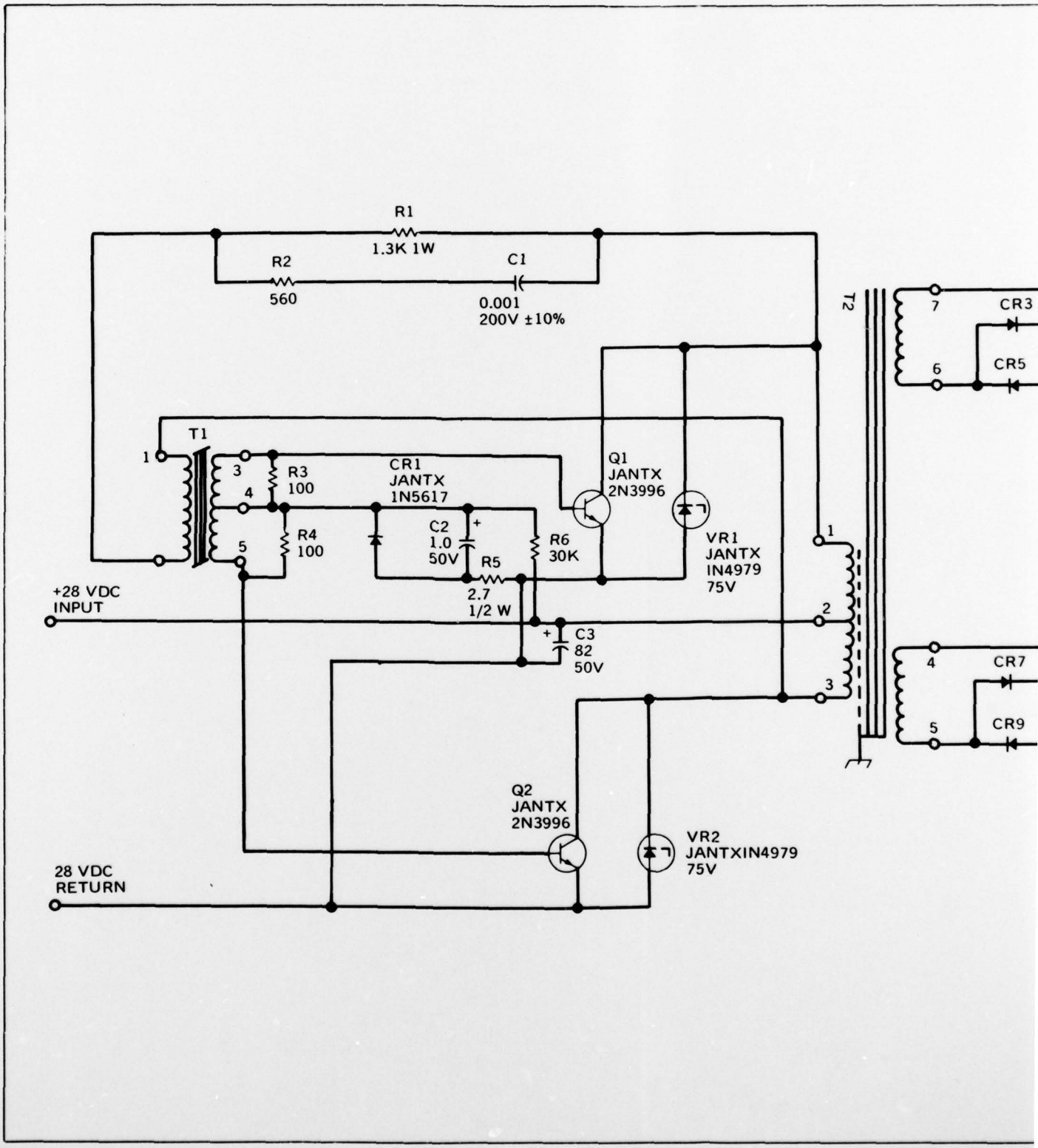


Figure 9. Pulse Top Clipper Regulator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R2
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C1
0.001
200V ±10%
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T2
CR3
CR5
CR7
CR9
R3
100
R4
100
CR1
JANTX
1N5617
C2
1.0
50V
R5
2.7
1/2 W
R6
30K
Q1
JANTX
2N3996
VR1
JANTX
IN4979
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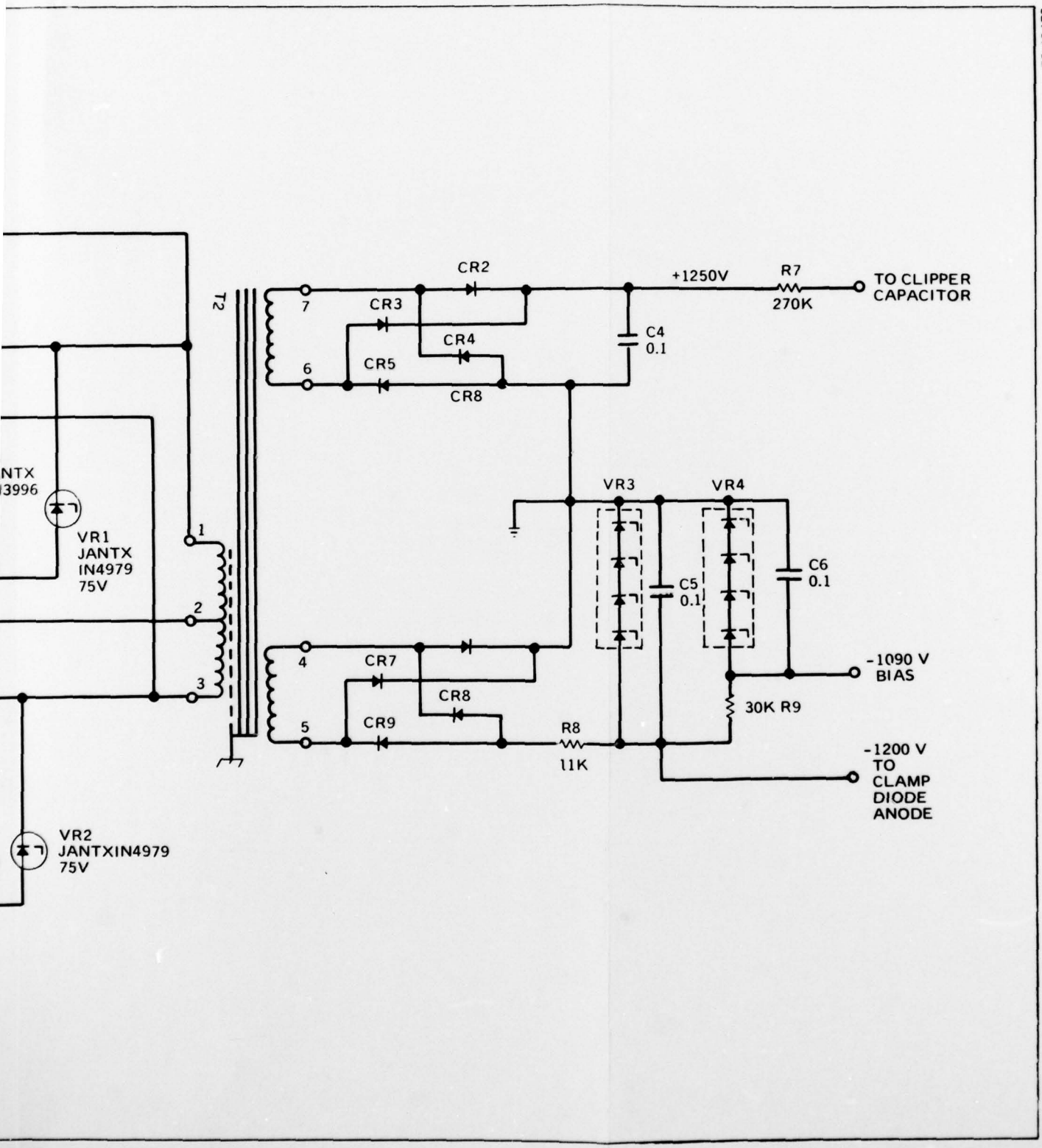
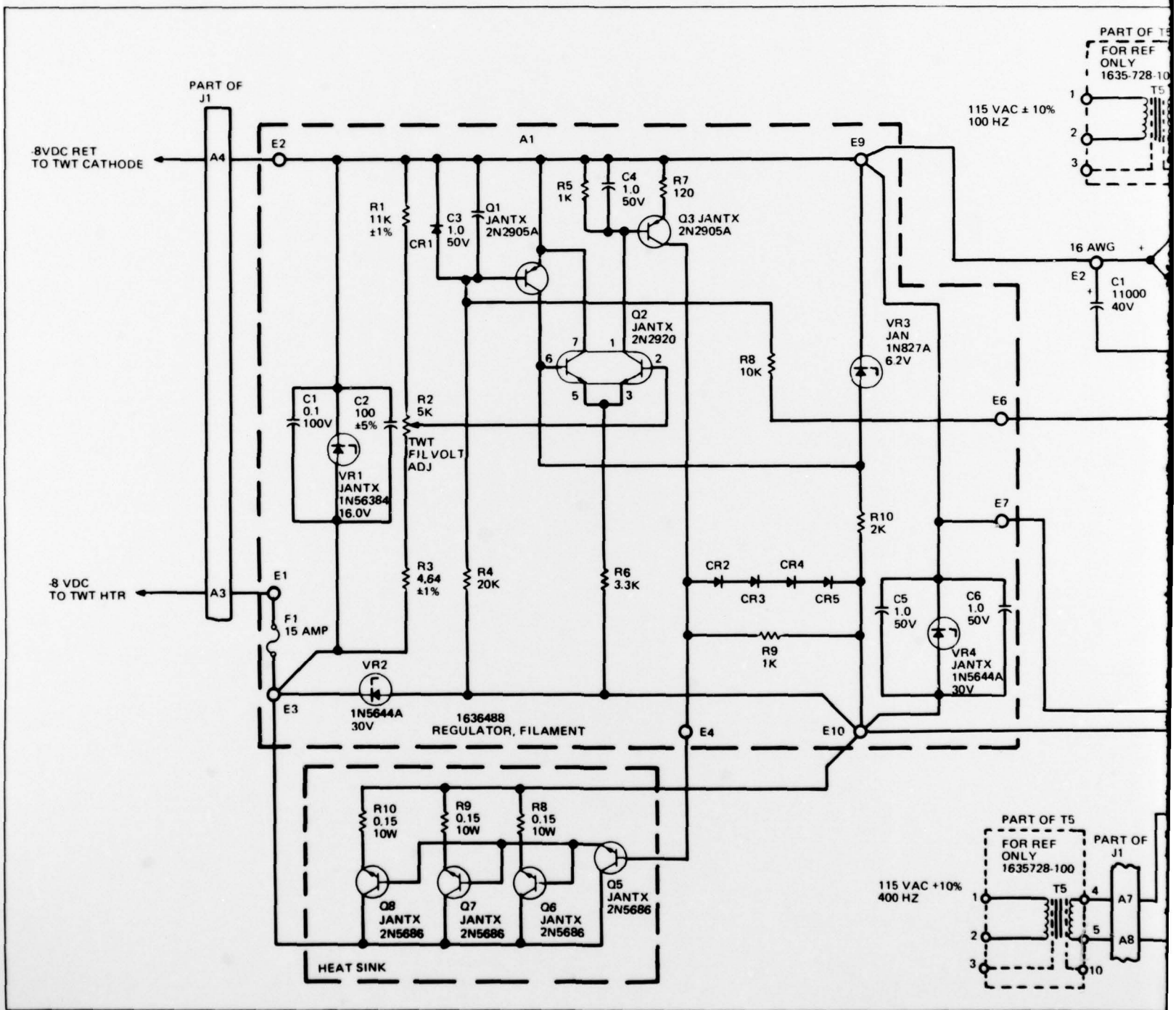


Figure 10. Bias, Clamp and Pulse Top Regulator Power Supply Circuits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-8VDC RET TO TWT CATHODE
A4
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115 VAC ± 10% 100 HZ
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16 AWG
E2
C1 11000 40V
R1 11K ±1%
CR1
C3 1.0 50V
Q1 JANTX 2N2905A
R5 1K
C4 1.0 50V
R7 120
Q3 JANTX 2N2905A
Q2 JANTX 2N2920
VR3 JAN 1N827A 6.2V
R8 10K
C1 0.1 100V
C2 100 ±5%
R2 5K
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VR1 JANTX 1N5638A 16.0V
E6
E7
R10 2K
-8 VDC TO TWT HTR
A3
E1
F1 15 AMP
R3 4.64 ±1%
R4 20K
R6 3.3K
CR2
CR4
CR3
CR5
C5 1.0 50V
C6 1.0 50V
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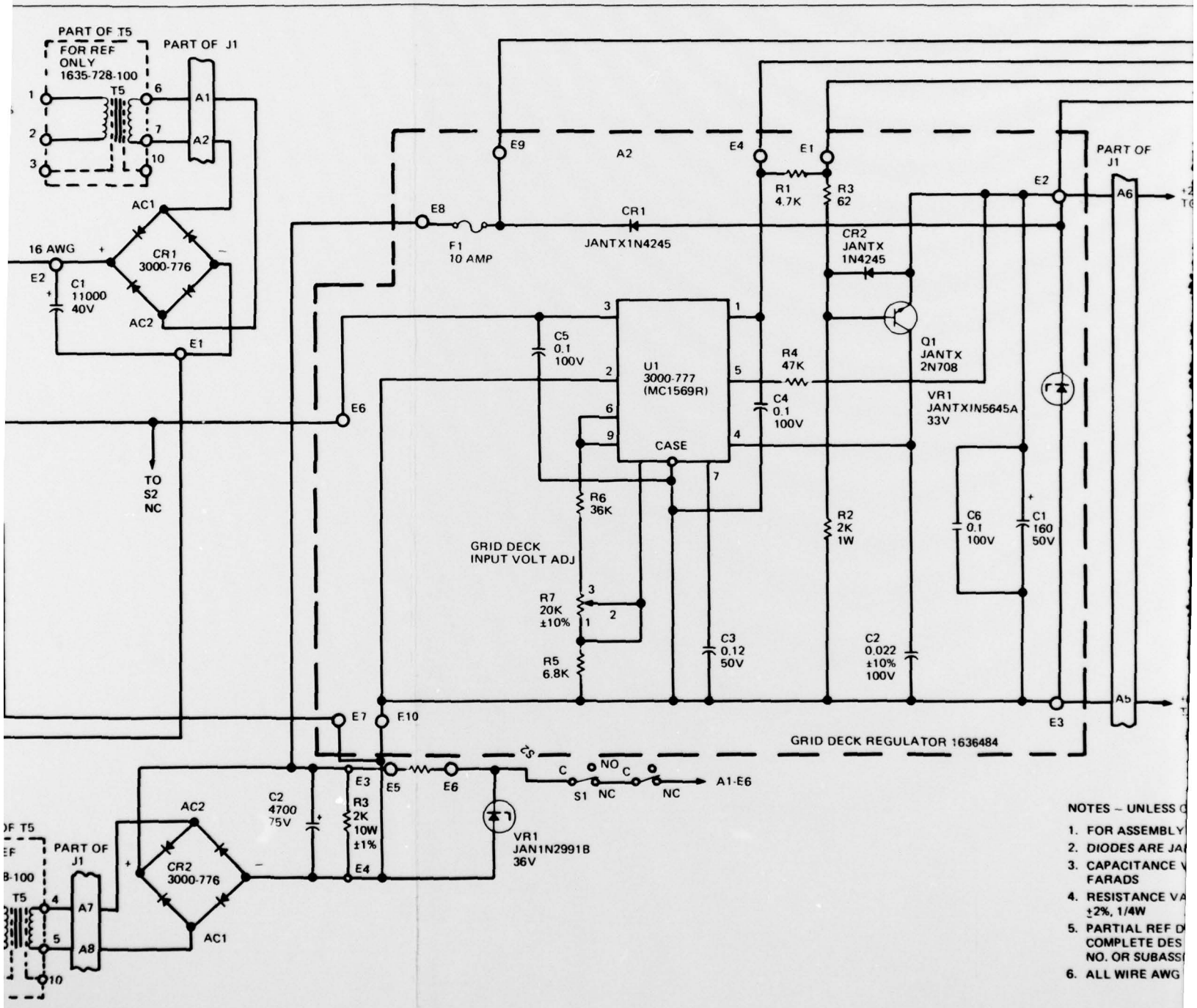

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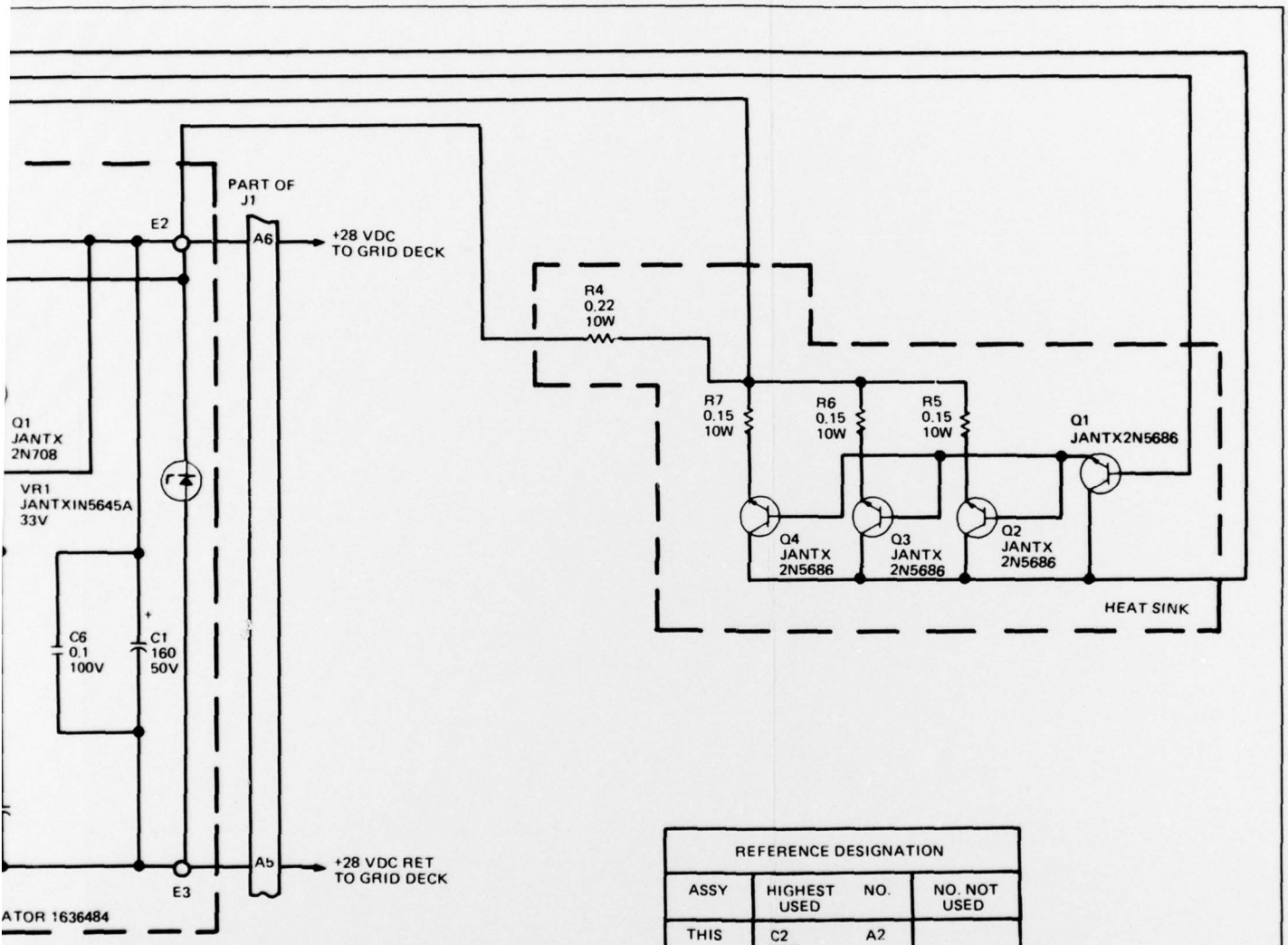

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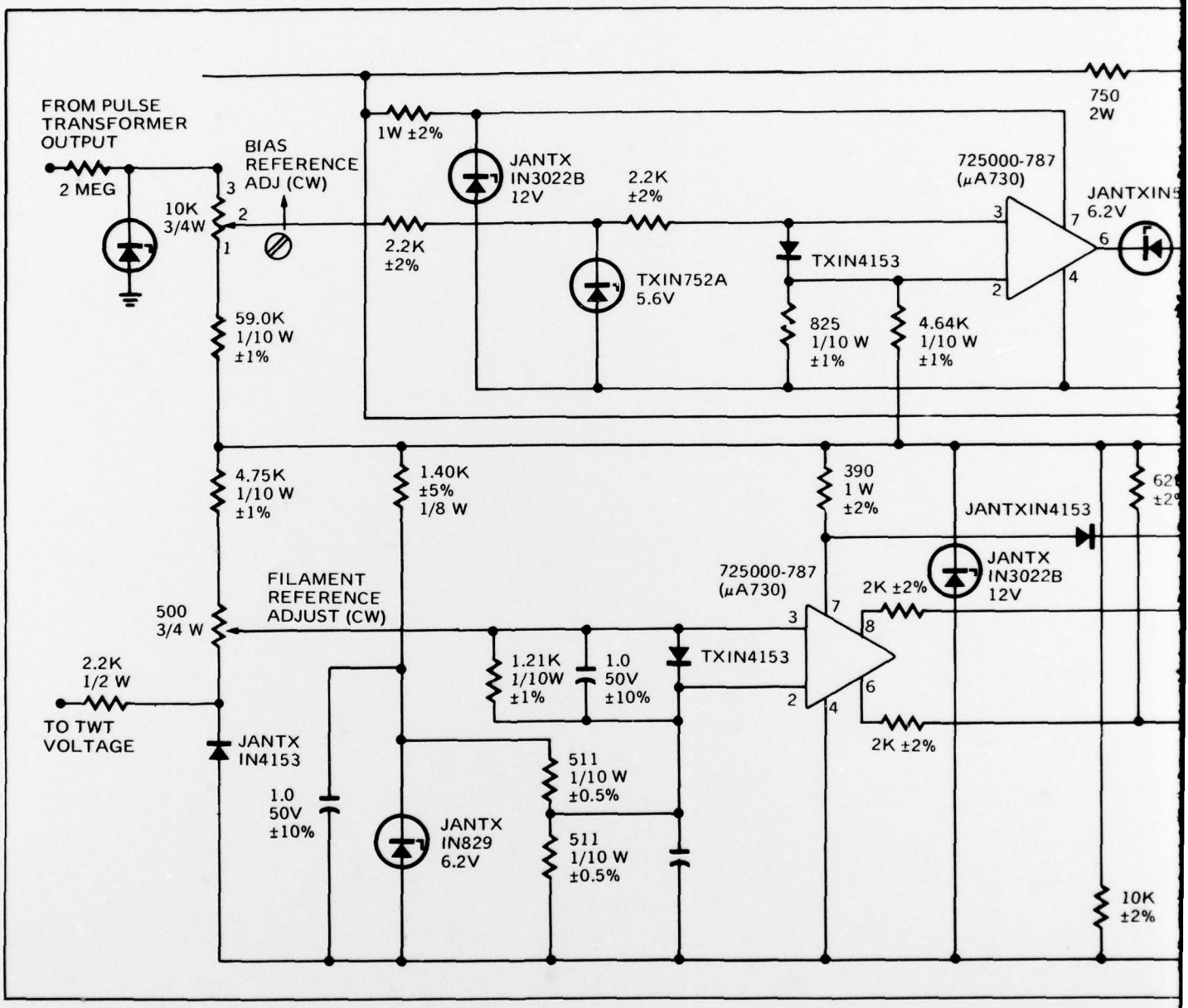
5. PARTIAL REF DES ARE SHOWN. FOR COMPLETE DES PREFIX WITH UNIT NO. OR SUBASSEMBLY DES
6. ALL WIRE AWG 18

Figure 11. Floating Deck Power Supplies

3


FROM PULSE TRANSFORMER OUTPUT
2 MEG
10K 3/4W
BIAS REFERENCE ADJ (CW)
59.0K 1/10 W ±1%
1W ±2%
JANTX IN3022B 12V
2.2K ±2%
2.2K ±2%
TXIN752A 5.6V
725000-787 (μA730)
TXIN4153
825 1/10 W ±1%
4.64K 1/10 W ±1%
750 2W
JANTXIN5
6.2V
4.75K 1/10 W ±1%
1.40K ±5% 1/8 W
390 1 W ±2%
JANTXIN4153
FILAMENT REFERENCE ADJUST (CW)
500 3/4 W
725000-787 (μA730)
JANTX IN3022B 12V
2K ±2%
2.2K 1/2 W
TO TWT VOLTAGE
1.21K 1/10W ±1%
1.0 50V ±10%
TXIN4153
JANTX IN4153
511 1/10 W ±0.5%
1.0 50V ±10%
JANTX IN829 6.2V
511 1/10 W ±0.5%
2K ±2%
10K ±2%

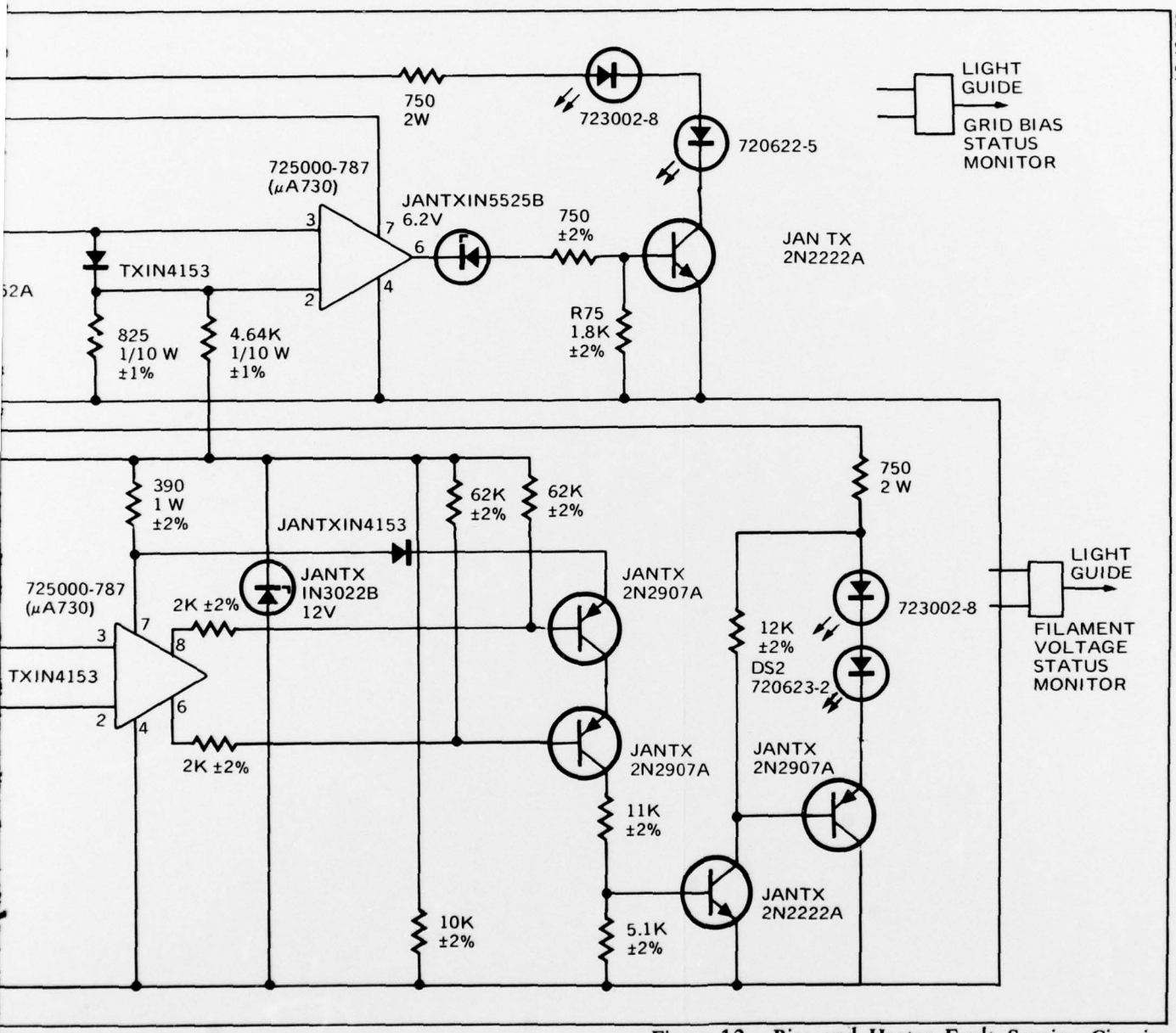


Figure 12. Bias and Heater Fault Sensing Circuits

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